CLAIMS

What is claimed is:

1. A device that comprises:

a plurality of circuits coupled together by asynchronous links, wherein the plurality of circuits includes a master circuit, and

wherein the master circuit is configured to send a first synchronization signal to one or more of the plurality of circuits, and

wherein each circuit that receives the first synchronization signal is configured to responsively send a second synchronization signal to one or more of the plurality of circuits.

2. The device of claim 1 wherein one of the plurality of circuits is configured to transmit and receive packets to and from external sources.

3. The device of claim 1 wherein one of the plurality of circuits is configured to manipulate data stored in another one of the plurality of circuits.

4. The device of claim 1 wherein one or more of the plurality of circuits is configured to store packet portions.

5. The device of claim 1 wherein the first synchronization signal comprises a value from a word counter coupled to the master circuit.

6. The device of claim 1 wherein the first synchronization signal comprises a relative value of a word counter coupled to the master circuit.

7. The device of claim 1 wherein the second synchronization signal comprises a value from a word counter coupled to one of the plurality of circuits.

8. The device of claim 7 wherein the first synchronization signal comprises a relative value of a word counter coupled to the master circuit.

9. The device of claim 1 wherein the first synchronization signal is sent in response to one or both of a system reset and a power-on procedure.

10. The device of claim 1 wherein the second synchronization signal is sent in response to a hot-plug insertion of a circuit.

11. The device of claim 1 wherein each one of the plurality of circuits that receives the first synchronization signal sets a word counter coupled to the circuit to a value based on an adjustment of a value indicated by the first synchronization signal and an upper bound of a round-trip latency between two of the plurality of circuits.

12. The device of claim 11 wherein the upper bound of the round trip latency is related to a deterministic and a nondeterministic delay.

13. The device of claim 1 wherein each one of the plurality of circuits that receives the second synchronization signal is configured to adjust the delays of one or more first-in-first-out (FIFO) data structures that are coupled to the circuit that received the second synchronization signal and responsively send a third synchronization signal to one or more of the plurality of circuits, wherein each one of the plurality of circuits that receives the third synchronization signal adjusts the delays of one or more FIFO data structures that are coupled to the circuit that received the third synchronization signal.

14. The device of claim 1 wherein each circuit, except the master circuit, that receives the second synchronization signal sets a word counter coupled to the circuit to a value based on a value indicated by the second synchronization signal.

15. A method comprising:

sending a first synchronization signal from a master circuit to a second circuit;

setting a word counter coupled to the second; and

sending a second synchronization signal from the second circuit to the master circuit or a third circuit.

16. The method of claim 15 wherein the first synchronization signal comprises a value from a word counter coupled to the master circuit.

17. The method of claim 15 wherein the first synchronization signal comprises a signal indicating a relative value of a word counter coupled to the master circuit.

18. The method of claim 15 wherein the second synchronization signal comprises a value from a word counter coupled to the second circuit.

19. The method of claim 15 wherein setting the word counter further comprises obtaining a value related to an upper bound of a round-trip latency between the first and second circuits.

20. The method of claim 15 wherein sending of the first synchronization signal occurs in response to one or both a system reset and a power-on procedure.

21. The method of claim 15 wherein each circuit that receives the first synchronization signal sets a word counter coupled to the circuit to a value based on an adjustment of a value indicated by the first synchronization signal and an upper bound of a round-trip latency between two of the plurality of circuits.

22. The method of claim 21 wherein the upper bound of the round trip latency is related to a deterministic and a nondeterministic delay.

23. A Fibre Channel (FC) fabric comprising:
a plurality of FC switches coupled together,
wherein at least one of the FC switches includes: a plurality of circuits coupled together by asynchronous links, wherein the plurality of circuits includes a master circuit, and wherein the master circuit is configured to send a first synchronization signal to one or more of the plurality of circuits, and wherein each circuit that receives the first

synchronization signal is configured to responsively send a second synchronization signal to one or more of the plurality of circuits.

24. The fabric of claim 23 wherein one of the plurality of circuits is configured to transmit and receive packets to and from external sources.

25. The fabric of claim 23 wherein one of the plurality of circuits is configured to manipulate data stored in another one of the plurality of circuits.

26. The fabric of claim 23 wherein one or more of the plurality of circuits is configured to store packet portions.

27. The fabric of claim 23 wherein the first synchronization signal comprises a value from a word counter coupled to the master circuit.

28. The fabric of claim 23 wherein the first synchronization signal comprises a relative value of a word counter coupled to the master circuit.

29. The fabric of claim 23 wherein the second synchronization signal comprises a value from a word counter coupled to one of the plurality of circuits.

30. The fabric of claim 29 wherein the first synchronization signal comprises a relative value of a word counter coupled to the master circuit.

31. The fabric of claim 23 wherein the first synchronization signal is sent in response to one or both of a system reset and a power-on procedure.

32. The fabric of claim 23 wherein each one of the plurality of circuits that receives the first synchronization signal sets a word counter coupled to the circuit to a value based on an adjustment of a value indicated by the first synchronization signal and an upper bound of a round-trip latency between two of the plurality of circuits.

33. The fabric of claim 32 wherein the upper bound of the round trip latency is related to a deterministic and a nondeterministic delay.

34. The fabric of claim 23 wherein each one of the plurality of circuits that receives the second synchronization signal is configured to adjust the delays of one or more first-in-first-out (FIFO) data structures that are coupled to the circuit that received the second synchronization signal and responsively send a third synchronization signal to one or more of the plurality of circuits, wherein each one of the plurality of circuits that receives the third synchronization signal adjusts the delays of one or more FIFO data structures that are coupled to the circuit that received the third synchronization signal.

35. The device of claim 23 wherein each one of the plurality of circuits, except the master circuit, that receives the second synchronization signal sets a word counter coupled to the circuit to a value based on a value indicated by the second synchronization signal.

36. The fabric of claim 23 wherein the second synchronization signal is sent in response to a hot-plug insertion of a circuit.

37. A network comprising:

at least two nodes; and

a Fibre Channel (FC) fabric coupling the nodes,

wherein the fabric comprises a plurality of FC switches coupled together, at least one of the FC switches includes: a plurality of circuits coupled together by asynchronous links, wherein the plurality of circuits includes a master circuit, and wherein the master circuit is configured to send a first synchronization signal to one or more of the plurality of circuits, and wherein each circuit that receives the first synchronization signal is configured to responsively send a second synchronization signal to one or more of the plurality of circuits.

38. The network of claim 37 wherein one of the plurality of circuits is configured to transmit and receive packets to and from external sources.

39. The network of claim 37 wherein one of the plurality of circuits is configured to manipulate data stored in another one of the plurality of circuits.

40. The network of claim 37 wherein one or more of the plurality of circuits is configured to store packet portions.

41. The network of claim 37 wherein the first synchronization signal comprises a value from a word counter coupled to the master circuit.

42. The network of claim 37 wherein the first synchronization signal comprises a relative value of a word counter coupled to the master circuit.

43. The network of claim 37 wherein the second synchronization signal comprises a value from a word counter coupled to one of the plurality of circuits.

44. The network of claim 43 wherein the first synchronization signal comprises a relative value of a word counter coupled to the master circuit.

45. The network of claim 37 wherein the first synchronization signal is sent in response to one or both of a system reset and a power-on procedure.

46. The network of claim 37 wherein each one of the plurality of circuits that receives the first synchronization signal sets a word counter coupled to the circuit to a value based on an adjustment of a value indicated by the first synchronization signal and an upper bound of a round-trip latency between two of the plurality of circuits.

47. The network of claim 46 wherein the upper bound of the round trip latency is related to a deterministic and a nondeterministic delay.

48. The network of claim 37 wherein each one of the plurality of circuits that receives the second synchronization signal is configured to adjust the delays of one or more first-in-first-out (FIFO) data structures that are coupled to the circuit that received the second synchronization signal and responsively send a third synchronization signal to one or more of the plurality of circuits, wherein each one of the plurality of circuits that receives the third synchronization signal adjusts the delays of one or more first-in-first-out (FIFO) data structures that are coupled to the circuit that received the third synchronization signal.

49. The device of claim 37 wherein each circuit, except the master circuit, that receives the second synchronization signal sets a word counter coupled to the circuit to a value based on a value indicated by the second synchronization signal.

50. The network of claim 37 wherein the second synchronization signal is sent in response to a hot-plug insertion of a circuit.